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06ES33

Third Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Two motors M_1 and M_2 are controlled by three sensors S_3, S_2 and S_1. One motor M_2 is to run any time all three sensors are ON(true). The other motor is to run whenever sensors S_2 or S_1, but not both are ON and S_3 is OFF. For all sensor combinations where M_1 is ON, M_2 is to be OFF, except when all are OFF and then both sensors must be OFF. Generate truth table, and write the Boolean equations for both outputs. Also implement using logic gates. **(08 Marks)**

b. Convert the following equations in to their canonical Boolean forms :
X(SOP) = a'b + bc
Y(POS) = (a' + b) (b + c'). **(06 Marks)**

c. Simplify the following Boolean equation using Karnaugh map and implement using logic gates. $f(a, b, c, d) = \Sigma_m(0, 5, 8, 15) + dc(2, 7, 9, 10, 13)$. **(06 Marks)**

2 a. Minimize the following Boolean equation using Quine – McClustey method
$f(a, b, c, d) = \Sigma_m (2, 3, 4, 6, 10, 12, 14)$. **(12 Marks)**

b. Simplify the following Boolean equation using VEM method.
$f(w, x, y, z) = \Sigma_m(1, 5, 8, 9, 12, 13, 14)$. **(08 Marks)**

3 a. Realize a 2 : 4 decoder using logic gates. Also write the truth–table. **(08 Marks)**

b. Implement the following Boolean functions using 3 : 8 decoder :
$f_1(a, b, c) = \Sigma_m(0, 1, 3, 5, 7)$
$f_2(a, b, c) = \Sigma_m(1, 2, 4, 6)$. **(06 Marks)**

c. Design and implement an Octal – to – Binary encoder. **(06 Marks)**

4 a. Realize the following Boolean function using 4 : 1 MUX
$f(a, b, c) = \Sigma_m(0, 1, 5, 6, 7)$. **(08 Marks)**

b. Design a full adder circuit using only NAND gates. **(06 Marks)**

c. Realize a 1-bit comparator using logic gates. Write the truth table. **(06 Marks)**

PART – B

5 a. With a neat logic diagram and truth – table, explain the operation of SR – Latch. Discuss how SR latch can used as a switch debouncer. **(12 Marks)**

b. Discuss "Race – Around" condition. Explain how this problem can be overcome using Master – slave JK flip-flop. **(08 Marks)**

6 a. With function table and logic diagram, explain the following shift – register operations :
i) SISO (right – shift only) ii) PIPO. **(08 Marks)**

b. Explain Johnson counter, with circuit diagram and truth – table. **(06 Marks)**

c. Design a mod – 6 synchronous counter using JK flip – flops. **(06 Marks)**

7 a. Analyze the synchronous sequential circuit shown in Fig. Q7(a) below. **(14 Marks)**

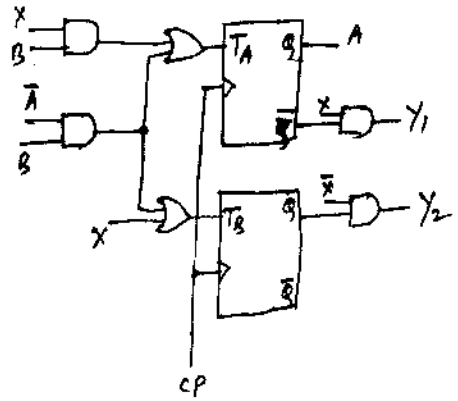

Fig. Q7(a)

b. Explain Moore and Mealy models for clocked synchronous sequential circuits. **(06 Marks)**

8 a. Design a synchronous counter for 4 → 6 → 7 → 3 → 1 → 4 - - - - . Avoid lockout condition. Use JK flip – flops. **(10 Marks)**

b. Obtain the transition table for the given state diagram and design the sequential network using JK flip – flops. **(10 Marks)**

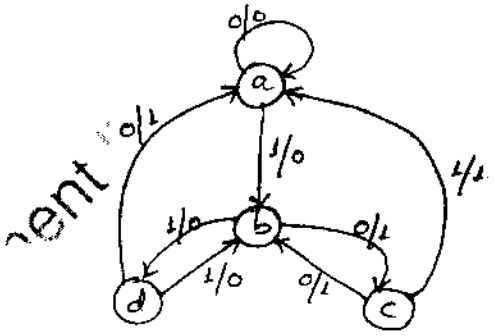

Fig. Q8(b)

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